**You have to submit this report via Moodle.**

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| Digital Design and Computer Architecture: Lab Report | | |
| Lab 3: Verilog for Combinational Circuits | | |
| Date | 09.04.2021 | Grade |
| Names | Berner, Zheng |  |
|  |  | Lab session / lab room |
|  |  | Friday 08:15  Zoom breakout room 60 |

**Use a zip file or tarball that contains the report and any other required material. Only one member from each group should submit the report. All members of the group will get the same grade.**

**The name of the submitted file should be *Lab3\_LastName1\_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.**

**Note 1: Please include all the required material. No links/shortcuts are accepted.**

**Note 2: The deadline for the report is a hard deadline and it will not be extended.**

**Exercise 1. Turning off the Redundant Displays**

If you do not like seeing all 7-segment displays showing the same number four times you may want to turn off the three extra 7-segment displays. They can be disabled by connecting their activation input to logic-1 (note that the activation input is active-low). In order to achieve this, you can add a new 4-bit output AN[3:0] into your top module and assign logic-1 to AN[1], AN[2] and AN[3], and logic-0 to AN[0].

At this point, you need to update the constraints file in order to map these new output signals to the activation pins on the board.

Do this by adding the following lines to your constraints file:

set\_property PACKAGE\_PIN U2 [get\_ports {AN[0]}]

set\_property PACKAGE\_PIN U4 [get\_ports {AN[1]}]

set\_property PACKAGE\_PIN V4 [get\_ports {AN[2]}]

set\_property PACKAGE\_PIN W4 [get\_ports {AN[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {AN}]

You can name the new output as you prefer. Just be careful to be consistent with your choice when updating the constraints file. After this little tweak, generate the programming file again and reprogram the board. You should now see only the right-most 7-segment display on.

**Exercise 2. Choosing a Specific Display**

Change your design of Exercise 1, so that you can select which 7-segment display to turn on. Design a decoder that 1) receives two inputs from two switches on the board and 2) based on them, activates only one of the 7-segment displays.

**Feedback**

If you have any comments about the exercise please add them here: mistakes in the text, difficulty level of the exercise, or anything that will help us improve it for the next time.